Systematic Approach for Scaling Coefficients of Discrete-Time and Continuous-Time Sigma-Delta Modulators

N. Beilleau, H. Aboushady, M. M. Louërat Université Paris VI, Laboratoire LIP6/ASIM 4 Place Jussieu, 75252 Paris Cedex 05, France Email: Nicolas.Beilleau@lip6.fr, Hassan.Aboushady@lip6.fr

Abstract—In this paper we present a systematic method to scale the integrators output swings of $\Sigma\Delta$ modulator. It is shown that this scaling method preserves both the Noise Transfer Function and the Signal Transfer Function of the modulator. Examples are given to illustrate the effectiveness of the proposed method to alleviate circuit non-idealities.

I. INTRODUCTION

Nowadays oversampled $\Sigma\Delta$ modulators [1] are the most commonly used A/D converters to achieve a high-level precision and are more and more developed in Continuous-Time (CT), Fig.1, for several advantages compared to the Discrete-Time (DT) modulators. There has been a lot of work on the coefficients determination in DT [2] and in CT [3][4] but they only took into account the system level design and the stability of the Noise Transfer Function (NTF). When it comes to circuit implementation, these coefficients must be scaled in order to limit the signal swing at the output of the integrators. This problem has already been considered in discrete-time $\Sigma\Delta$ modulators [5][6][7].

In this paper, we present an easy and systematic approach to scale DT and CT $\Sigma\Delta$ modulators. It will be shown that in the case of CT $\Sigma\Delta$, the coefficients of the modulator can also be scaled to reduce the effect of some circuit non-idealities. In section II., we present the scaling method which allows to limit the integrator output swing. In section III. we demonstrate the efficiency of the method with two different continuous-time $\Sigma\Delta$ architectures and how this method can be used to increase the circuit performance. The conclusion is given in the section IV.

II. DESCRIPTION OF THE METHOD

In the following we assume that the DT coefficients are given using R. Schreier toolbox [8] and are transformed to CT using the technique described in [4]. The NTF is optimized to reduce the quantization noise power in the signal band while ensuring the stability of the modulator by placing the NTF poles inside the root locus unit circle.



(a) Feedback arhitectures



(b) Feedforward architectures

Fig. 1. Scaling method for feedback(a) and feedforward(b) $\Sigma\Delta$ architectures.

A. Scaling

The idea behind this scaling method is to preserve the same NTF :

$$NTF = \frac{1}{1 + H_{DAC}H_d} \tag{1}$$

where H_d is loop filter and H_{DAC} is the feedback DAC filter, Fig.2. To keep a general meaning we did not precise the domain.

From equation (1) we can see that only H_d determines the NTF because H_{DAC} is not considered in the scaling procedure. Therefore to conserve the NTF all the scaling factors f_i , introduced to scale the integrators output swings, have to disapear in H_d final expression. To respect this condition we have to do the following :

i. divide i^{th} integrator gain by the scaling factor f_i .



Fig. 2. A general model of a $\Sigma\Delta$ modulator with the open-loop filter $(H_c(s))$, the loop filter $(H_d(s))$ and the feedback DAC filter $(H_{DAC}(s))$.

ii. distribute f_i in such away to be canceled in H_d final expression.

As shown in Fig.1 the distribution of the scaling factors depends on the $\Sigma\Delta$ architecture. We take into account both Feed-Back (FB) and FeedForward (FF) architectures.

B. The last integrator

We can see in Fig.1 that the last integrators are not scaled. In fact, scaling these integrators would imply adding a new gain, increasing the complexity of the circuit implementation. For the FB architectures the output of the last integrator is determined with the design of the NTF. In the case of the Schreier toolbox [8] this signal is scaled for the quantizer input. For the FF architectures the last coefficient is introduced in the last integrator gain. This coefficient scales the integrator output swing.

C. STF conservation

A consequence of the conservation of the NTF is the conservation of the STF :

$$STF = \frac{H_c}{1 + H_{DAC}H_d}$$

with H_c open loop filter, Fig.2. For the FF architectures H_c is the inverse of H_d . For the FB architectures we demonstrate in the following the conservation of H_c . We consider a scaled signal $\frac{u_i(s)}{f_{i-2}}$ at the point A in the Fig.1(a) and we determine the signal $w_i(s)$ at the point B of the same figure :

$$\begin{split} w_i(s) &= \left[\frac{u_i(s)}{f_{i-2}} - w_i(s)\frac{g_j f_i}{f_{i-2}}\right] \frac{f_{i-2}}{sT f_{i-1}} \frac{f_{i-1}}{sT f_i} \\ &= \left[u_i(s) - w_i(s)g_j f_i\right] \frac{1}{(sT)^2} \frac{1}{f_i} \\ w_i(s) &= \frac{u_i(s)}{(sT)^2 - g_j} \frac{1}{f_i} \end{split}$$

If $w_i(s)$ is an intermediate signal the scaling factor f_i will be canceled by the next integrator. If $w_i(s)$ is the last integrator output we eliminate f_i because the last integrator is not scaled. In both cases there is no scaling factor in the final expression



(a) original coefficients



(b) seared coefficients

Fig. 3. Integrators swings decrease

of H_c . The same reasoning can be applied to the CIFB without the g_j term. Although shown here for CT $\Sigma\Delta$ this demonstration is also valid for DT $\Sigma\Delta$ modulators.

D. Simulations and values

 $\Sigma\Delta$ modulators are non-linear systems due to the quantizer in the loop. Therefore, in pratical, behavioural simulations are used to determine the f_i value [5][6][7]. We consider an ideal model with a sinusoidal input which has a frequency in the bandwidth and the peak SNR amplitude. We determine f_i starting at the first integrator:

1. the starting value for all the scaling factors is 1, $f_1 = f_2 = \dots = f_n = 1$

- 2. simulate the CT $\Sigma\Delta$ modulator with the previously determined scaling factors and the others left to 1.
- 3. the scaling factor, f_i , corresponding to the i^{th} simulation is calculated using the following expression :

$$f_i = \frac{max(output \ i^{th} \ integrator)}{desired \ i^{th} \ integrator \ output \ swing}$$

4. repeat steps 2 and 3 until i=order.

The value of the desired output depends on system and circuit levels choices and can be different for each integrator.

III. EXAMPLES

We have implemented this scaling method in a $\Sigma\Delta$ behavioural simulator and we consider continuous-time $\Sigma\Delta$ of which NTFs were determined in DT with the Schreier toolbox [8] and were transformed to CT with modified z-transform method [4]. The simulation models are ideal and just have saturations at the integrators output.

In order to show the several advantages of using the proposed scaling method, we will study 2 different examples. In the first example we are just looking for reducing the output integrators swing, subsection A., and in a second case we demonstrate that the scaling method may be used to increase the linearity of the modulator, subsection B.

A. CT 6th order Bandpass $\Sigma\Delta$

First we consider a CT 6th order 1-bit Bandpass $\Sigma\Delta$ modulator with its original coefficients. In Fig.3(a) most of the integrators would overload in circuit implementation. The 5th and the 1st integrators are the most critical. In order to decrease the swings we apply the previously described method. We scale the integrators output swings to 0.6 (Normalized to $\frac{1}{V_{REF}}$). In Fig.3(b) we can see that the 5th and the 1st integrators output swings are obviously attenuated.

On the other hand, to study the effect of scaling on the Signal to Noise Ratio (SNR), the 2 $\Sigma\Delta$ modulators having the coefficients listed in tables I,II have been simulated with the output of the integrators being saturated to +1 and -1. From Fig.4 we can clearly see that while the SNR of the $\Sigma\Delta$ using the original coefficients is significantly degraded, the SNR of the scaled coefficients is identical to the $\Sigma\Delta$ without saturation.

To illustrate the STF conservation we can see in Fig.5 the NTF and the STF which have not been affected by the scaling factors.

B. 3rd order CIFB 1-bit

The first integrator of the $\Sigma\Delta$ is the most critical, its performances affect directly those of the modulator. In the specific case of a current-mode CT $\Sigma\Delta$ modulator [9], the non-linearity of the first integrator can be reduced by changing its gain. The scaling method presented in this paper allows to adjust this gain



Fig. 4. 6th order CRFF, OSR=64, points=16384, $f_{input} = \frac{13}{f_{sampling}}$





TABLE I Original Coefficients

| A_{int_1} | A_{int_2} | A_{int_3} | A_{int_4} | A_{int_5} | A_{int_6} |
|-------------|-------------|-------------|-------------|-------------|-------------|
| 1 | 1 | 1 | 1 | 1 | 0.1617 |
| a_1 | a_2 | a_3 | a_4 | a_5 | a_6 |
| 0.4931 | -0.6431 | -0.3038 | -0.4578 | -0.0672 | 1 |

TABLE II Scaled Coefficients

| A_{int_1} | A_{int_2} | A_{int_3} | A_{int_4} | A_{int_5} | A_{int_6} |
|-------------|-------------|-------------|-------------|-------------|-------------|
| 0.2796 | 1.4261 | 0.6898 | 1.4822 | 0.2127 | 1.2066 |
| 1 | | | | | |
| a_1 | a_2 | a_3 | a_4 | a_5 | a_6 |



Fig. 6. Comparison between ideal system-level $\Sigma\Delta$ simulation and circuit level simulation.

| | A_{int_1} | A_{int_2} | A_{int_3} |
|---------------|-------------|-------------|-------------|
| 1st scaling | 0.2167 | 0.2560 | 0.7929 |
| final scaling | 0.0433 | 1.2801 | 0.7929 |
| | a_1 | a_2 | a_3 |
| 1st scaling | 1 | 0.2560 | 1.4192 |
| final scaling | 1 | 0.2838 | 1.0086 |

TABLE III linearity improvemen

without changing the NTF. An optimization loop has been implemented to adapt the gain of the first integrator following the results from circuit simulation.

Fig.6 shows the result of such an optimization for a third-order continuous-time $\Sigma\Delta$ modulator where the resulting coefficients are listed in table III. We can clearly see the large amplitude of the third harmonic for the first simulation done with coefficients scaled for maximum signal swing ($A_{int_1} = 0.216$). After several iterations, we find a suitable value ($A_{int_1} = 0.043$) which attenuates the third harmonic and gives a SNR very close to the ideal SNR.

IV. CONCLUSION

In this paper we have presented an efficient and systematic scaling method for FB and FF architectures of CT and DT $\Sigma\Delta$ modulators. In order to insure the stability of the system this method preserves the initial NTF. We demonstrated that the NTF conservation implies the STF conservation for the architectures discussed here. In one example, we have seen how scaling can significantly reduce SNR degradation due to integrators output swing limitation. In the other example, we have shown that reducing the output swing of the 1st integrator can be used to reduce harmonic distortion of a 3rd order CIFB $\Sigma\Delta$ modulator.

REFERENCES

- J.C. Candy and G.C. Temes. "Oversampled Delta-Sigma Data Converters". IEEE Press, 1992.
- [2] R. Schreier. "An empirical study of high-order single-bit delta-sigma modulators". *IEEE Trans. Circuit and Sys.* 2, CAS-40:461–466, August 1993.
- [3] R. Schreier and B. Zhang. "Delta-Sigma Modulators Employing Continuous-Time Circuitry". *IEEE Trans. Circuit and Sys. 1*, CAS-43:324–332, April 1996.
- [4] H. Aboushady and M.M. Louërat. "Systematic approach for discrettime to continuous-time tranformation of sigma-delta modulators". In *ISCAS'02*, May 2002.
- [5] B. Boser and B. Wooley. "The design of Sigma-Delta Modulation Analog-to-Digital Converters". *IEEE J. Solide-State Circuits*, vol. 23, Dec. 1988.
- [6] Kirk C-H Chao, Shujaat Nadeem, Wai L Lee, and Charles G. Sodini. "A higher order topology for interpolative modulators for oversampling A/D converters". *IEEE Trans. Circuit and Sys.*, CAS-37:309–318, 1990.
- [7] Zhi-Ming Lin and Wen-Huei Sheu. "A generic multiple-feedback architecture and method for the design of high-order Sigma-Delta modulators". *IEEE Trans. Circuit and Sys.* 2, CAS-49:465–473, July 2002.
- [8] R. Schreier. "The Delta-Sigma Toolbox for MATLAB". Oregon State University, November 1999.
- [9] H. Aboushady, F. Montaudon, F. Paillardet, and M.-M. Louërat. "A 5mW, 100kHz, Current-Mode Continuous-Time Sigma-Delta Modulator with 84dB Dynamic Range". *European Solid-State Circuits Conference*, pages 283–286, September 2002.